CLAIMS

What is claimed is:

1. A JTAG-compliant chip for communicating with a non-JTAG-compliant chip comprising:

a JTAG-compliant test access port (TAP) controller;

a plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip; and

a controller connected to:

receive signals from a shift register, and

in response to the signals from the shift register and the TAP controller, send and receive signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip.

2. The JTAG-compliant chip of Claim 1 wherein the JTAG-compliant chip is a programmable logic device and the controller is configured from logic in the programmable logic device.

3. The JTAG-compliant chip of Claim 1 wherein the TAP controller accesses external TDI and TDO control signals.

4. The JTAG-compliant chip of Claim 3 wherein the TAP controller allows the controller to access the external TDI and TDO control signals.

5. The JTAG-compliant chip of Claim 1 wherein the controller comprises:

a shift register connected to external TDI and TDO control signals; and

a state machine that in response to commands in the shift register sends and receives signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip.

6. The JTAG-compliant chip of Claim 1 wherein the controller uses the signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip to write to and read from the non-JTAG-compliant chip.

7. The JTAG-compliant chip of Claim 6 wherein the non-JTAG-compliant chip is a flash memory chip and the controller further uses the signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip to erase the flash memory chip.

8. The JTAG-compliant chip of Claim 2 wherein the programmable logic device is a field programmable gate array chip.

9. A method of using a programmable chip having a boundary scan structure to access a chip not having a boundary scan structure comprising:

programming the chip having the boundary scan structure to implement a controller for:

receiving boundary scan input signals,

providing boundary scan output signals,

providing signals to the chip not having a boundary scan structure, and

receiving signals from the chip not having a boundary scan structure.

10. The method of Claim 9 wherein the step of providing signals to the chip not having a boundary scan structure comprises providing commands to indicate one of a plurality of operations to be performed.

11. The method of Claim 10 wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing an address to the chip not having a boundary scan structure.

12. The method of Claim 11 wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing data to the chip not having a boundary scan structure.

13. The method of Claim 9 wherein the step of receiving signals from the chip not having a boundary scan structure comprises receiving data from the chip not having a boundary scan structure addressed by some of the signals provided in the step of providing signals to the chip not having a boundary scan structure.

14. A method of configuring a non-JTAG chip from a JTAG-compliant chip having core logic, the method comprising the steps of:

a. loading an instruction into a JTAG TAP interface of the JTAG-compliant chip that causes the JTAG TAP interface to enable a path for serial data to go from a JTAG-compliant TDI pin to the core logic of the JTAG-compliant chip;

b. defining a shift register in the core logic of the JTAG-compliant chip that receives data transferred from the TDI pin; and

c. defining a controller that receives the shift register data in parallel and generates from this data signals applied to pins of the JTAG-compliant chip that are connected to pins of the non-JTAG chip.

15. The method of Claim 14 wherein the shift register defined in the core logic of the JTAG-compliant chip outputs data to a JTAG-compliant TDO pin.

16. The method of Claim 14 comprising the additional step performed by the controller of receiving signals from the non-JTAG chip.

17. The method of Claim 14 wherein the shift register comprises two shift registers, one of which receives address data for addressing part of the non-JTAG chip and another of which receives data words for being loaded into the non-JTAG chip.

18. The method of Claim 14 wherein the shift register receives both address data for addressing part of the non-JTAG chip and data words for being loaded into the non-JTAG chip.

19. The method of Claim 18 wherein the address data is loaded into the shift register first, and becomes a starting address for subsequent data words to be loaded into the non-JTAG chip, and is incremented internally by the controller for loading a plurality of the data words.

20. The method of Claim 18 wherein the address data, data word, and any other data needed by the non-JTAG chip are applied in parallel to the non-JTAG chip.

21. The method of Claim 20 wherein the address data, data word, and any other data needed by the non-JTAG chip configure part of the non-JTAG chip.